WHAT IS CLAIMED IS:

1. An instruction retirement system of a superscalar microprocessor which executes a program comprising a set of instructions having a predetermined program order, said retirement system for simultaneously retiring groups of instructions executed in or out of order by the microprocessor, said retirement system comprising:

(a) a first means for monitoring the status of the instructions to determine which instruction or instructions have been executed;

(b) a second means, coupled to said first means, for determining whether each executed instruction is retirable;

(c) a temporary buffer for storing results of instructions executed out of program order;

(d) a register array, coupled to said temporary buffer, for storing retirable-instruction results; and

(e) a third means, coupled to said second means, said temporary buffer, and said register array,

(i) for retiring a group of said instructions determined by said second means to be retirable, by simultaneously transferring their results from said temporary buffer to said register array, and

(ii) for retiring instructions executed in order by storing their results directly in said register array.

2. The system of claim 1, wherein said second means includes further means for determining that an instruction is retirable by checking whether there are no unexecuted instructions appearing earlier in the program order, and said retirable-instruction results are the execution results of the instructions determined to be retirable.

3. The system of claim 1, wherein:

said first means includes further means for assigning done flags to the instruction or instructions determined to have been executed by said first means; and

said second means includes still further means for checking said done flags to determine whether all instructions appearing earlier in the program order have completed to thereby determine whether each executed instruction is retirable.

4. The system of claim 1, further comprising:

(f) selection logic means coupled to said temporary buffer and said register array and responsive to said third means, for:

(i) receiving the results of the retirable group of instructions from said temporary buffer and transferring the results to said register array responsive to control signals from said third means; and

(ii) receiving the results of the instructions executed in order and storing the results directly in said register array responsive to further control signals from said third means.

5. The system of claim 1, further comprising selection logic for selecting and latching results to be transferred from said temporary buffer to said register array.

6. The system of claim 1, wherein said third means retires the group of instructions in a single clock cycle.

7. The system of claim 6, wherein the group comprises at least 2 instructions.

8. The system of claim 7, wherein the group comprises 4 instructions.

9. The system of claim 1, further comprising:

(f) tag assignment means for generating one or more tags to specify the location of results in said temporary buffer based on data dependencies determined by comparing the addresses of the source register field of each instruction to the addresses of the destination register fields of the other instructions in the set of instructions.

10. The system of claim 9, wherein said temporary buffer comprises:

(i) a plurality of storage locations for storing the results of the instructions executed out of program order according to said tags generated by said tag assignment means;

(ii) a plurality of address ports coupled to said plurality of storage locations, for receiving said tags to thereby address said plurality of storage locations to store the results;

(iii) a plurality of input ports coupled to said plurality of storage locations, for receiving the results to be stored in said temporary buffer;

(iv) a first plurality of output ports coupled to said plurality of storage locations for outputting the results to said register array; and

(v) a second plurality of output ports coupled to said plurality of storage locations for outputting the results to one or more functional units in the superscalar microprocessor.

11. The system of claim 10, wherein said temporary buffer includes further means for storing results of instructions completed in the program order.

12. An method for retiring instructions in a superscalar microprocessor which executes a program comprising a set of instructions having a predetermined program order, said method for simultaneously retiring groups of instructions executed in or out of order by the microprocessor, comprising the steps of:

(1) monitoring the status of the instructions using a first means to determine which instructions or instructions have been executed;

(2) for determining whether each executed instruction is retirable using a second means;

(3) storing results of instructions executed out of program order in a temporary buffer;

(4) storing retirable-instruction results in a register array, coupled to said temporary buffer; and

(5) retiring a group of said instructions determined by said second means to be retirable, by simultaneously transferring their results from said temporary buffer to said register array using a third means which is coupled to said second means, said temporary buffer, and said register array; and

(6) retiring instructions executed in order by storing their results directly in said register array.

13. The method of claim 12, further comprising the step of determining that an instruction is retirable by checking whether there are no unexecuted instructions appearing earlier in the program order, and said retirable-instruction results are the execution results of the instructions determined to be retirable.

14. The method of claim 12, further comprising the steps of:

assigning done flags to the instruction or instructions determined to have been executed by said first means; and

checking said done flags to determine whether all instructions appearing earlier in the program order have completed to thereby determine whether each executed instruction is retirable.

15. The method of claim 12, further comprising the steps of:

(7) receiving the results of the retirable group of instructions from said temporary buffer and transferring the results to said register array responsive to control signals from said third means using a selection logic means coupled to said temporary buffer and said register array and responsive to said third means; and

(8) receiving the results of the instructions executed in order and storing the results directly in said register array responsive to further control signals from said third means.

16. The method of claim 12, further comprising the steps of selecting and latching results to be transferred from said temporary buffer to said register array.

17. The method of claim 12, further comprising the step of retiring the group of instructions in a single clock cycle.

18. The method of claim 17, further comprising the step of retiring at least 2 instructions in a single clock cycle.

19. The method of claim 18, further comprising the step of retiring 4 instructions in a single clock cycle.

20. The method of claim 12, further comprising the step of:

(7) generating one or more tags to specify the location of results in said temporary buffer based on data dependencies determined by comparing the addresses of the source register field of each instruction to the addresses of the destination register fields of the other instructions in the set of instructions using a tag assignment means.

21. The method of claim 20, further comprising the steps of:

(8) receiving said tags to thereby address a plurality of storage locations to store the results in said temporary buffer; and

(9) storing the results of the instructions executed out of program order according to said tags in said plurality of storage locations in said temporary buffer.

22. The method of claim 21, further comprising the step of outputting the results stored in said plurality of storage locations to said register array.

23. The method of claim 21, further comprising the step of outputting the results stored in said plurality of storage locations to one or more functional units in the superscalar microprocessor.

24. The method of claim 21, further comprising the step of storing results of instructions completed in the program order in said temporary buffer.